

Serial No.: 10/798,846

REMARKS

Claims 1-30 are pending in the application. Claims 15, 18, 21, 23, 26 and 29 have been amended herein. Favorable reconsideration of the application, as amended, is respectfully requested.

I. ALLOWABLE SUBJECT MATTER

Applicants note with appreciation the indicated allowability of claims 15-30 subject to being amended to overcome any indefiniteness rejection. As is discussed below, claims 15, 18, 21, 23, 26 and 29 have been amended to address the indefiniteness issue raised by the Examiner. Accordingly, claims 15-30 should now be in condition for allowance.

II. REJECTION OF CLAIMS 15-30 UNDER 35 USC §112, 2nd ¶

Claims 15-30 stand rejected under 35 USC §112, second paragraph, as being indefinite. Withdrawal of the rejection is respectfully requested for at least the following reasons.

Regarding claims 15 and 23, the Examiner indicates that it is unclear in the claims what "a first method" and "a second method" are referring to in the apparatus and method claims, respectively.

Applicants note that the "first method" in claim 15 refers to the particular type of arithmetic operation performed on the recited operands. Similarly, the "second method" refers to the particular type of arithmetic operation performed on the recited operands in each instance. See, for example, the description in the Specification at Page 31, Lines 26-30; and Page 32, Line 33 to Page 33, Line 5. In the cited text, the first method is said to be, for example, addition whereas the second method is, for example, subtraction.

In order to better clarify such understanding, applicants have amended claims 15, 18, 21, 23, 26 and 29 to refer more simply to a "first arithmetic operation" and a "second arithmetic operation", respectively.

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Kunisa et al. describes a digital modulation circuit which inputs a data stream to convert to a channel bit stream. Fig. 5, reproduced above, illustrates how data is input at terminal 10 and is RS encoded by an RS encoder 13. The RS encoded data is input and stored in a memory 15. In addition, the RS encoded data is input to a j-type EX-OR unit 20. The j-type EX-OR unit 20 includes a data generator j-types of conversion 25. The data generator 25 provides j-types of RS codes for scrambling to a first EX-OR unit 21. The data output from the RS encoder 13 undergoes encoding with each of the j scrambling codes. A comparator 23 determines which scrambling pattern provides the minimum absolute value DSV. Based on the determination of the comparator 23, the data generator 25 outputs to the second EX-OR unit 31 the scrambling patterning giving the minimum DSV. The scrambling pattern is then used to further encode the data previously stored in the memory 15 via the second EX-OR unit 31, RLL encoder 33 and the NRZI modulator 35.

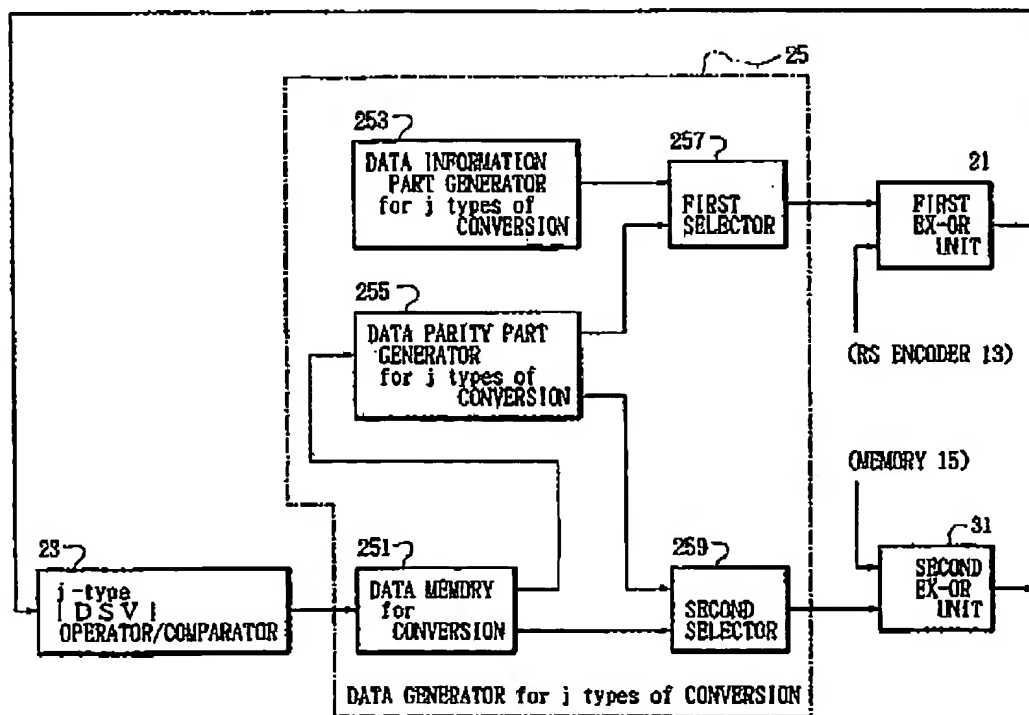


Fig. 6 of Kunisa et al.

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Fig. 6 illustrates the data generator 25 in more detail. A data information part generator 253 provides for j-types of conversion of the data; whereas the data parity part generator 255 provides for the j-types of conversion for the j parity parts.

Consequently, *Kunisa et al.* does teach converting data and generating corresponding parity parts j-different ways by virtue of the data generator 25 in order to determine which particular pattern results in the minimum DSV. *However, it is by virtue of the pattern which produces the minimum DSV that the data is subsequently encoded.*

Claims 1 and 8 refer to encoding N pieces of information by applying to each of the N pieces of information one corresponding scrambling pattern among the M scrambling patterns so as to generate N pieces of scrambled information. It appears the Examiner is associating the j types of scrambling patterns from the data generator 20 in *Kunisa et al.* with the M scrambling patterns recited in claims 1 and 8 (i.e., j = M). However, claims 1 and 8 refer to each of the N pieces of information being scrambled with one corresponding scrambling pattern among the M scrambling patterns. In *Kunisa et al.* each piece of information (i.e., data input to terminal 10) is scrambled by all of the j scrambling patterns so as to generate M pieces of scrambled information. The scrambling pattern providing the minimum DSV is identified, and the remaining M-1 pieces of scrambled information are discarded.

Thus, the present invention as recited in claims 1 and 8 provides for a plurality (between 2 and N) of pieces of information being generated by using only one from a total of M scrambling patterns. This is in stark contrast to *Kunisa et al.* in which a plurality (j) of scrambled codes are used to generate one (smallest DSV) scrambled code.

Accordingly, *Kunisa et al.* neither teaches nor suggests the scrambling of data as recited in claims 1 and 8. Moreover, *Kunisa et al.* does not teach or suggest the features as set forth in the various dependent claims 2-7 and 9-14. For at least these reasons, withdrawal of the rejections is respectfully requested.

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IV. CONCLUSION


Accordingly, all claims 1-30 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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